AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Currently Amended*) A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library comprising ~~containing~~ connection information ~~on a plurality of circuits~~ and delay time information for a ~~on rises and falls of each input terminal and output terminal of said~~ plurality of circuits,

wherein, for at least one of said plurality of circuits, said library further comprises ~~contains~~ logical operation information representing correspondence between a logical value of each input terminal of said at least one circuit and a ~~the~~ logical value of each ~~the~~ output terminal of said at least one circuit ~~at least one of said plurality of circuits~~, and said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit, and

~~wherein,~~ when making a delay analysis of the logic circuit comprising said at least one circuit ~~including at least one of said plurality of circuits~~, a delay time is selected from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit ~~a logic operation of said circuit~~.

2. (*Currently Amended*) A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising ~~containing~~ connection information ~~on a plurality of circuits~~ and delay time information for a ~~on rises and falls of each input terminal and output terminal of said~~ plurality of circuits,

wherein, for at least one of said plurality of circuits, said library further comprises ~~contains~~ logical operation information representing correspondence between a logical value of each input terminal of said at least one circuit and a logical value of each ~~the~~ output terminal of said at least one circuit ~~at least one of said plurality of circuits~~, and said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit, and

~~wherein,~~ when making a delay analysis of a logic circuit, a delay time between an ~~the~~ input terminal and an ~~the~~ output terminal of said at least one circuit is selected from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit ~~a logic operation of said circuit~~.

3. (*Currently Amended*) A method for making a delay analysis of a logic circuit, comprising the steps of:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising ~~containing~~ connection information, ~~on a plurality of circuits,~~ delay time information ~~on rises and falls of each input terminal and output terminal of at least one of said plurality of circuits,~~ and logic operation information representing correspondence between a logical value of each input

terminal and a logical value of each ~~the~~ output terminal of at least one of said plurality of circuits, said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit; and

if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit ~~of said circuits~~ from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit ~~a specified logic operation of said circuit~~.

4. (*Currently Amended*) A computer-readable medium having stored thereon a program for executing:

(a) a process step comprising:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising ~~containing~~ connection information ~~on a plurality of circuits~~, delay time information ~~on rises and falls of each input terminal and output terminal of each one of said plurality of circuits,~~ and logic operation information representing correspondence between a logical value of each input terminal and a logical value of each ~~the~~ output terminal of each one of said plurality of circuits, said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit; and

if a logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit ~~of said circuits~~ from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit ~~a logic operation of said circuit~~; and

(b) a process step of performing a delay calculation using said selected delay time as a propagation delay time of said at least one circuit ~~of circuits~~.